GX5292 SERIES

3U PXI HIGH SPEED DYNAMIC DIGITAL I/O CARD

- 32 input / output channels, dynamically configurable on a per channel basis
- 256 MB of on-board vector memory
- Supports 1.5 V, 1.8 V, 2.5 V, 3.3 V, and 5 V TTL/LVTTL interfaces
- Supports LVDS, M-LVDS, LVDM interfaces
- 100 MHz vector rate
- Stimulus / Response & Real-Time Compare modes
- Operates as a stand-alone card or with up to seven additional synchronous slave boards

DESCRIPTION

The GX5292 is a high performance, cost-effective 3U PXI dynamic digital I/O board offering 32 TTL or LVDS input or output channels with dynamic direction control. The GX5292 supports deep pattern memory by offering 256 MB of on-board vector memory with dynamic per pin direction control and with test rates up to 100 MHz. The single board design supports both master and slave functionality without the use of add-on modules.

FEATURES

The GX5292 supports selectable I/O levels of 1.5 V, 1.8 V, 2.5 V, or 3.3 V (TTL, LVTTL, CMOS, and LVCMOS compatible). In addition, the GX5292 supports 32 differential channels for LVDS, M-LVDS, or LVDM logic families. The TTL/LVTTL interface utilizes a programmable voltage source, which sets the output logic levels from 1.4 V to 3.6 V. Programmable thresholds of 1.5V, 1.8V, 2.5V or 3.3V (5V compatible) are supported for input signals. Recommended operating input voltage range is from 0 V to 5.5 V.

A windowing method is utilized for PCI memory accesses, which limits the required PCI memory space for each board to only 16MB, thus preserving test system resources. A direct mode, for continuous data transfer between the test system controller and the I/O pins of the GX5292 is also supported.

The GX5292 offers 256 MB of vector memory, with 64 Mb per channel. Programmable I/O width allows trading vector width for vector depth. Under software control, the GX5292's vector memory can be configured to support channel widths of 32, 16, 8, 4, 2 and 1 with corresponding vector depths of 64 Mb, 128 Mb, 256 Mb, 512 Mb, 1024 Mb, and 2048 Mb.

The GX5292 provides programmable TTL/LVTTL output clocks and strobes, and supports external clock and strobe. A programmable PLL (phase locked loop) provides configurable clock frequencies and delays. An LVDS output clock is also provided.

The GX5292's sequencer can halt or pause on a defined address or loop through the entire memory as well as loop on a defined address range or through a defined block of memory. Two modes of digital test are also supported – a Stimulus / Response and a Real-Time Compare mode. The Stimulus / Response mode is used for driving and capturing data. Alternatively, for digital tests requiring long test vectors, the Real-Time Compare mode can be used to significantly shorten overall test times by comparing in real-time, expected test results and logging only failed vectors and resultant test results (pass or fail).

SOFTWARE

The GX5292 is supplied with DIOEasy, which provides powerful graphical vector development / waveform display tools as well as a virtual instrument panel, 32-bit DLL driver libraries, and documentation. The virtual panel can be used to interactively control and monitor the instrument from a window that displays the instrument's current settings and status. In addition, various interface files provide access to the instrument's function library for programming tools and languages such as ATEasy, Microsoft® and Borland® C/C++, Microsoft Visual Basic®, Borland Delphi, and LabVIEW.

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Optionally, DtifEasy is available for use with the GX5292. DtifEasy offers a complete LASAR post-processor and test execution environment for post-processing and executing of LASAR generated .tap files.

APPLICATIONS

- Automatic Test Equipment (ATE)
- Semiconductor test
- Displays, printers, and disk drive testing
- ASICs testing
- A/D and D/A testing
- Video acquisition / playback applications
- High speed, bi-directional bus testing / emulation

SPECIFICATIONS

INPUT / OUTPUT CHANNEL FEATURES	
LOGIC FAMILIES	TTL/LVTTL/CMOS/LVCMOS (1.5 V, 1.8 V, 2.5 V, 3.3 V, or 5 V), LVDS/LVDM/M-LVDS
I/O LEVELS	TTL/LVTTL/CMOS/LVCMOS: Programmable Output Voltage Level 1.4 V (Min); 3.6 V (Max) Input Threshold 1.5 V, 1.8V, 2.5V, or 3.3 V (5V tolerant) Recommended Operating Conditions 0V (Min); 5.5V (Max) LVDS/LVDM/M-LVDS: Recommended Operating Conditions Voltage Output: -1.4V (Min.); 3.8 V (Max.) Voltage Input: .05V (Min.); 3.3V (Max.)
CHANNEL TIMING SKEW	1 ns same card, 1 ns between cards
NUMBER OF CHANNELS	32 I/O, direction and configuration is dynamically configurable on a per vector and per channel basis
MEMORY DEPTH PER CHANNEL	64Mb - 2Gb
TEST MODES	
STIMULUS / RESPONSE	Drive / Capture data, up to 64 Mb per channel
REAL-TIME COMPARE	Drive / compare data against expected data pattern Expect & mask data on a per cycle basis
REAL TIME COMPARE RECORD MEMORY	1024 x 64 bits of record memory Records compared data and address
REAL TIME COMPARE STOP MODES	Stop on defined count errors (max is 1024) Stop when detected failures equal the defined number of failures Stop on defined comparison data value Stop on defined program counter value
TIMING	
INTERNAL TEST CLOCK (PLL)	
FREQUENCY RANGE	5 Hz (Min.); 100 MHz (Max.)
ACCURACY	Greater of (+/- 1Hz or +/- 0.02% of programmed value) + accuracy of reference clock (PXI 10 MHz or external reference clock)
JITTER	+/- 20 mUI of internal clock frequency, max
REFERENCE	PXI 10 MHz clock or XClk (external clock) input
INTERNAL B CLOCK OUTPUT (TTL/LVTTL)	
FREQUENCY RANGE	300 KHz (Min.); 100 MHz (Max.)
ACCURACY	Greater of (+/- 1Hz or +/- 0.5% of programmed value) + accuracy of reference clock)
INTERNAL C CLOCK OUTPUT (LVDS/LVDM/MOLVDS)	
FREQUENCY RANGE	300KHz (Min.); 100 MHz (Max.)
ACCURACY	Greater of (+/- 1Hz or +/- 0.5% of programmed value) + accuracy of reference clock)
EXTERNAL TEST CLOCK INPUT	
FREQUENCY RANGE (CONFIGURED AS SAMPLE CLOCK)	0 Hz (Min.); 100 MHz (Max.)
FREQUENCY RANGE (CONFIGURED AS INPUT TO PLL)	8 MHz (Min.); 10.5 MHz (Max.)
PULSE WIDTH	40% Min, 60% Max
INPUT LEVEL	User selectable I/O level: 1.5 V, 1.8 V, 2.5 V, or 3.3 V (5 V tolerant)
EXTERNAL STROBE CLOCK INPUT	
FREQUENCY RANGE	0 Hz (Min.); 100 MHz (Max.)
LOGIC LEVELS	TTL / LVTTL / CMOS / LVCMOS Input threshold: 1.5 V, 1.8 V, 2.5 V, or 3.3 V (5V tolerant)
EXTERNAL STATUS & CONTROL SIGNALS	
LOGIC LEVELS	TTL/LVTTL/CMOS/LVCMOS: Prog. Output Voltage Level: 1.4 V (Min); 3.6 V (Max) Input Threshold: 1.5 V, 1.8V, 2.5V, or 3.3 V (5V tolerant)
TRIGGER SOURCE	Software, PXI trigger bus, External event, External trigger input (overrides Run command)
EXTERNAL CLOCK ENABLE	Internal (software), External input (via J3 connector)
EXTERNAL STROBE ENABLE	Internal (software), External input (via J3 connector)
EXTERNAL EVENT BUS	16 input lines with mask and logic AND conditioning
PAUSE	External pause input overrides Pause command
PAUSE LATENCY	10 clock cycles to acquire data after pause deasserts
RUN	Run status indicator (J3 connector)
POWER	
3.3 VDC	200 mA (Min.); 4 A (Max.)
5 VDC	50 mA (Min.); 2 A (Max.)
12 VDC	.03mA (Min.); .1mA (Max.)

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SPECIFICATION

ENVIRONMENTAL	
OPERATING TEMPERATURE	0 to 50° C
STORAGE TEMPERATURE	-20° C to 70° C
SIZE	3U PXI
WEIGHT	200 g
FRONT PANEL CONNECTORS	
J1	I/O TTL Signals, 68-pin VHD connector
J2	I/O LVDS Signals, 68-pin VHD connector
J3	Timing Signals, 68-pin VHD connector
J4	Control Connector, 68-pin VHD connector

Note: Specifications are subject to change without notice.

ORDERING INFORMATION

GX5292	100 MHz Digital I/O Board with 256 MB of vector memory and LVDS levels
ACCESSORIES	
GT95014	Connector interface, SCSI to 100 Mil Grid, Single Ended I/F Board
GT95015	Connector Interface for all 5xxx/35xx, SCSI to 100 Mil Grid, differential
GT95021	2' shielded cable (68-pin SCSI)
GT95022	3' Shielded cable (68-pin SCSI)
GT95028	10' Shielded cable (68-pin SCSI)
GT95031	6' Shielded cable (68-pin SCSI)

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